AMENDMENTS TO THE CLAIMS

1. (Original) An integrated capacitor comprising:

a semiconductor substrate;

an outer vertical plate laid over the semiconductor substrate, the outer vertical plate consisting of a plurality of first conductive slabs connected vertically using multiple first via plugs, wherein the outer vertical plate defines a grid area;

an inner vertical plate laid over the semiconductor substrate in parallel with the first vertical plate and encompassed by the grid area defined by the outer vertical plate, wherein the inner vertical plate consisting of a plurality of second conductive slabs connected vertically using multiple second via plugs; and

a horizontal conductive plate laid under the outer vertical plate and inner vertical plate over the semiconductor substrate for shielding the outer vertical plate from producing a plate-to-substrate parasitic capacitance thereof;

wherein the inner vertical plate is electrically connected with the horizontal conductive plate using at least one third via plug.

2. (Original) The integrated capacitor of claim 1 wherein the horizontal conductive plate is floating and is made of metal.

3. (Original) The integrated capacitor of claim 1 wherein the horizontal conductive plate and the overlaying outer vertical plate are isolated from each other by at least one

layer of dielectric material.

4. (Original) The integrated capacitor of claim 1 wherein both of the first conductive slab and the second conductive slab are made of metal.

5. (Original) The integrated capacitor of claim 1 wherein the outer plate and the inner vertical plate are electrically isolated from each other.

6. (Original) The integrated capacitor of claim 1 wherein when the outer vertical plate is electrically connected to a node A, the inner vertical plate is electrically connected to a node B, and the semiconductor substrate is grounded, the plate-to-substrate parasitic capacitance is produced at the node B.

7. (Original) The integrated capacitor of claim 6 wherein when the outer vertical plate is electrically connected to a node A, the inner vertical plate is electrically connected to a node B, and the semiconductor substrate is grounded, there is no plate-to-substrate parasitic capacitance produced at the node A.

8. (Original) A method of forming an electrically polar integrated capacitor, comprising the steps of:

providing a semiconductor substrate comprising an outer vertical plate consisting of a plurality of first conductive slabs connected vertically using multiple first via plugs, and an inner vertical plate consisting of a plurality of second conductive slabs connected vertically using multiple second via plugs, wherein

the outer vertical plate defines a grid area, and the inner vertical plate is encompassed by the grid area defined by the outer vertical plate;

providing a conductive plate under the outer vertical plate and the inner vertical plate on the semiconductor substrate for shielding the outer vertical plate from producing a plate-to-substrate parasitic capacitance thereof; and

electrically connecting the inner vertical plate with the conductive plate using at least one third via plug.

9. (Original) The method of claim 8 wherein the conductive plate is floating and is made of metal.

10. (Original) The method of claim 8 wherein the conductive plate and the overlaying outer vertical plate are isolated from each other by at least one layer of dielectric material.

11. (Original) The method of claim 8 wherein when the outer vertical plate is electrically connected to a node A, the inner vertical plate is electrically connected to a node B, and the semiconductor substrate is grounded, the plate-to-substrate parasitic capacitance is produced at the node B.

12. (Original) The method of claim 8 wherein when the outer vertical plate is electrically connected to a node A, the inner vertical plate is electrically connected to a node B, and the semiconductor substrate is grounded, there is no plate-to-substrate parasitic capacitance produced at the node A.

13. (Currently amended) A method of forming an electrically polar integrated capacitor, comprising:
providing a semiconductor substrate;
providing a conductive plate on the semiconductor substrate, wherein the conductive plate is electrically isolated from the semiconductor substrate;
providing a plurality of first capacitor members and second capacitor members insulated from the first capacitor members over the conductive plate, wherein the first capacitor members define a grid area encompassing the second capacitor member to form an integrated capacitor; wherein each of the plurality of first capacitor members is isolated from the conductive plate by at least one layer of dielectric material;
electrically isolating the first capacitor members from the underlying conductive plate; and
electrically connecting the second capacitor members with the underlying conductive plate.

14. (Original) The method of claim 13 wherein each of the plurality of first or second capacitor members is a vertical plate consisting of a plurality of conductive slabs connected vertically using multiple via plugs.

15. (Original) The method of claim 13 wherein each of the plurality of first or second capacitor members is a vertical capacitor bar consisting of a plurality of conductive squares connected vertically using multiple via plugs.

16. (Original) The method of claim 13 wherein the first capacitor member and the second capacitor member are

arranged in a symmetric manner to form a matching capacitor unit.

17. (Canceled)

18. (Previously presented) The method of claim 13 wherein the conductive plate is floating and is made of metal.